PCT / IB 03 / 04290
19.09.03

Europäisches Patentamt
European Patent Office
Office européen des brevets



# Bescheinigung Certificate Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

**Patentanmeldung Nr. Patent application No. Demande de brevet n°**

02079336.0

**PRIORITY DOCUMENT**
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
Application no.: 02079336.0
Demande no:

Anmeldetag:
Date of filing: 18.10.02
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

Koninklijke Philips Electronics N.V.
Groenewoudseweg 1
5621 BA Eindhoven
PAYS-BAS

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

**Frequency-independent voltage divider**

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

H03H7/24

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SK TR

Frequency-independent voltage divider



The present invention relates to a voltage divider arrangement comprising a reference terminal, an input terminal for receiving an input signal with respect to the reference terminal, an output terminal for supplying an output signal with respect to the reference terminal, and a resistor arrangement arranged on a substrate and coupled between the input terminal and the reference terminal.

In such voltage divider arrangements, respective compensation capacitors are integrated to provide a frequency-independent voltage dividing function. Frequency-independent voltage dividers are known from the general state of the art. As an example, document US 6,100,750 discloses a frequency-independent voltage divider arrangement of the type defined in the opening paragraph, wherein a distributed compensation capacitor having one side coupled to the input terminal and having another side coupled to the resistor arrangement is provided in a distributed fashion. In particular, the distributed compensation capacitor is constituted by a conductor track of the resistor arrangement, a further conductor track which covers the conductor track at least partly and is coupled to the input terminal, and an insulator which isolates the conductor track electrically from the further conductor track.

Fig. 1 shows a schematic circuit diagram of the frequency-independent voltage divider. The resistor arrangement comprises a series arrangement of resistors with more than two resistors $R_1$ to $R_{M+1}$. An arbitrary node of the series arrangement can be loaded by a parasitic capacitor $CP_k$. A compensation capacitor $CCMP_k$ is coupled between the relevant arbitrary node and the input terminal arranged at the left side of the circuit diagram. Thus, the distributed parasitic capacitance CP of resistor R is compensated by a distributed compensation capacitance CCMP. In Fig. 1, it is assumed that the last node M+1 at the right side of the circuit diagram is connected to ground.

To achieve a frequency independent resistive behaviour, the capacitive voltage division on each node should exactly match the resistive voltage division. This means that for all k (k=1, 2, ...M) the following equation must be met:

$$\frac{CP_k}{CCMP_k} = \frac{R_1 + R_2 + \ldots + R_k}{R_{k+1} + R_{k+2} + \ldots + R_{M+1}} \quad [1]$$

If the above criterion is met, all the signal transfers from the input terminal to the nodes are frequency-independent of the input signal. Therefore, it is possible to couple a plurality of output terminals to a plurality of nodes in order to take off a plurality of output signals which are all frequency-independent.

In a practical embodiment, the frequency-independent voltage divider based on the above principle can be realised by means of an integrated resistor. In this case, the integrated resistor may be regarded as an infinite number of infinitesimal series connected resistors $R_1$ to $R_{M+1}$, where M approximates to infinity.

Fig. 2 shows a plan view of a folded integrated resistor 20 with a meandering shape as described in the above prior art. In order to satisfy the above criterion, a distributed compensation capacitance 10 is generated by forming a conductive layer 10 on top of the resistor arrangement 20 and separated by an insulation layer 30. The integrated resistor 20 is connected between the input terminal 2 and the reference terminal 1, while the distributed compensation capacitance 10 is also connected to the input terminal 2.

Fig. 3 shows a side view of this known frequency-independent voltage divider where the integrated resistor 20 is isolated from a substrate or handle waver 50 by a first insulator 40, and the compensation is made through the distributed compensation capacitance, e.g. a conductor track 10, isolated from the integrated resistor 20 by a second insulation layer 30. For low values of the index k, the ratio $CP_k/CCMP_k$ must approach to zero. This would mean that $CCMP_k$ should increase to infinity. However, this cannot be achieved due to the limited width of the body of the integrated resistor 20. Consequently, an inherent error is made in the compensation.

It is therefore an object of the present invention to provide a frequency-independent voltage divider arrangement, by means of which an improved compensation of the parasitic capacitance can be obtained.

This object is achieved by a voltage divider arrangement as claimed in claim 1.

Accordingly, a new way of constructing a frequency-independent voltage divider is proposed. The influence of parasitic capacitances is compensated by a compensation capacitance structure arranged between the resistor arrangement and the

substrate. This new way of construction offers a better compensation and opens new possibilities for the use of these voltage dividers in integrated circuit processes or situations where the known construction is not possible. Due to the fact that the compensation structure is located between the resistor and the substrate, the compensation structure shields the resistor partly from the substrate, and thus shields the parasitic capacitance. Whereas in the known distributed resistor, the parasitic capacitance of every segment of the resistor is equal, in the distributed resistor according to the invention the sum of the areas of the parasitic capacitance and the compensation capacitance is equal. This allows for better compensation, due to the fact that it is now possible to achieve a ratio between the parasitic capacitance and the compensation capacitance which approximates zero for low values of k.

The resistor arrangement may have a meandering shape and may be made of poly- silicon. The distributed compensation capacitance structure may comprise a conductor layer of predetermined shape, e.g. a triangular shape, and may be made of suitable conducting material, e.g. heavily doped silicon. Furthermore, the distributed compensation capacitance structure may be separated from the resistor arrangement and the substrate by respective insulation layers which may be made of suitable non-conducting material, e.g. of silicon oxide. This arrangement of the distributed compensation capacitance structure between the insulation layers provides as a further advantage depending on the applied IC processes that the insulation layers are able to withstand a larger voltage then in the known structure of the prior art.

Further advantageous developments are defined in the dependent claims.

In the following, the present invention will be described in greater detail based on a preferred embodiment with reference to the accompanying drawings in which:

Fig. 1 shows a schematic equivalent circuit diagram of a frequency-independent voltage divider;

Fig. 2 shows a plan view on a layout of a known frequency-independent voltage divider;

Fig. 3 shows a side view of the known frequency-independent voltage divider of Fig. 2;

Fig. 4 shows a side view of a frequency-independent voltage divider according to the preferred embodiment of the present invention;

Fig. 5 shows a plan view of the frequency-independent voltage divider according to the preferred embodiment; and

Fig. 6 shows a schematic cross-sectional side view of the frequency-independent voltage divider according to the preferred embodiment with connection terminals.

The preferred embodiment will now be described on the basis of an integrated voltage divider with a resistor arrangement 20 of a meandering shape.

Fig. 4 shows a side view of the frequency-independent voltage divider according to the preferred embodiment. Contrary to the known arrangement of Fig. 3, the distributed compensation capacitance structure 10 now shields the resistor arrangement 20 partly from the substrate 50. Thereby, the distributed parasitic capacitance is also shielded. While in the known design of Fig. 3, the parasitic capacitance of every segment of the resistor arrangement 20 is equal, now the sum of the areas of the parasitic capacitance $CP_k$ and the compensation capacitance $CCMP_k$ is equal. This allows for a better compensation, because it is now possible to achieve a ratio of $CP_k/CCMP_k$ approximating to zero for low values of k, which was not possible in the known designs, as $CCMP_k$ would have to increase to infinity.

To achieve optimum compensation, the width $D_k$ of the compensation layer of the distributed compensation capacitance structure must be determined for every k = 1, 2, ...M. To achieve this, it is assumed that the resistance of the resistor arrangement 20 is equal for every segment k, i.e. $R_1 = R_2 = \ldots = R_{M+1}$.

Furthermore $CP_k = CP_{sq} \cdot (DR - D_k) \cdot WR$, wherein $CP_{sq}$ is the parasitic capacitance per unit area of resistor, WR is the width of the resistor body of the resistor arrangement 20, DR is the length of one resistor segment or the width of the total resistor layout, and $D_k$ is the width of the compensation capacitance structure at segment k.

Consequently, the compensation capacitance can be calculated as follows:

$$CCMP_k = CCMP_{sq} \cdot D_k \cdot WR \qquad [2]$$

Based on equation [1] the following equation can be obtained:

$$\frac{CP_{sq} \cdot (DR - D_k)}{CCMP_{sq} \cdot D_k} = \frac{k}{M + 1 - k} \qquad [3]$$

From the above equation [3] the width of the compensation structure 10 can be calculated as follows:

$$D_k = \frac{DR}{1 + \frac{k}{M+1-k} \cdot \frac{CCMP_{sq}}{CP_{sq}}} \qquad [4]$$

The resulting shape of the compensation capacitance structure 10 corresponds to a triangular shape as indicated in Fig. 5. This compensation structure 10 is arranged between the resistor arrangement 20 and the substrate 50 and is separated by respective upper and lower insulation layers 30, 40. The upper insulation layer 30 and the lower insulation layer 40 may both be made e.g. of silicon oxide or another suitable non-conducting material. The compensation capacitance structure 10 may be made of heavily doped silicon or another suitable conduction material, and the resistor arrangement 20 may be made of poly-silicon.

Fig. 6 shows an equivalent diagram of the proposed frequency-independent voltage divider with respective connection terminals 1, 2, 3. At the meandering resistor arrangement 20, an input terminal 2, an output terminal 3 and a reference terminal 1 are provided, wherein the reference terminal 1 is connected to the substrate 50 and to electrical ground level. Furthermore, equivalent parasitic capacitances are schematically shown, whereby the shielding function of the compensation capacitance structure is made clear.

The proposed improved frequency-independent voltage divider can be specifically in high-frequency applications such as RGB amplifiers in television integrated circuits, radio frequency (RF) amplifiers, oscilloscope probes or the like.

It is noted that the present invention is not restricted to the above-preferred embodiment but can be used in any voltage divider arrangement where a distributed compensation capacitance structure is provided for compensating a distributed parasitic capacitance of a resistor arrangement. In particular, the resistor arrangement 20 and the compensation capacitance structure 10 may be provided with any shape suitable to obtain the required compensation, e.g. to satisfy the criterion set out in equation [1]. Moreover, any other suitable conductive material may be used for implementing the resistor arrangement 20 and the compensation capacitance structure. The preferred embodiment may thus vary within the scope of the attached claims.

CLAIMS:



1. A voltage divider arrangement comprising a reference terminal, an input terminal for receiving an input signal with respect to said reference terminal, an output terminal for supplying an output signal with respect to said reference terminal, and a resistor arrangement arranged on a substrate and coupled between said input terminal and said reference terminal, wherein a distributed compensation capacitance structure for compensating the influence of a distributed parasitic capacitance is arranged between said resistor arrangement and said substrate.

2. A voltage divider arrangement according to claim 1, wherein said resistor arrangement has a meandering shape.

3. A voltage divider arrangement according to claim 2, wherein said resistor arrangement is made of poly-silicon.

4. A voltage divider arrangement according to any one of the preceding claims, wherein said distributed compensation capacitance structure comprises a conductor layer of a predetermined shape.

5. A voltage divider arrangement according to claim 4, wherein said predetermined shape is a triangular shape.

6. A voltage divider arrangement according to claim 4 or 5, wherein the width of said conductor layer in the horizontal direction is selected according to the following equation:

$$D_k = \frac{DR}{1 + \frac{k}{M+1-k} \cdot \frac{CCMP_{sq}}{CP_{sq}}},$$

wherein $CP_{sq}$ denotes the parasitic capacitance per unit area of resistor, DR denotes the length of said resistor arrangement, k denotes an index of a segment of said transistor arrangement;

M denotes the total number of segments of said transistor arrangement, $CCMP_{sq}$ denotes the distributed compensation capacitance per unit area of resistor and $D_k$ denotes said width of said conductor layer.

7. A voltage divider arrangement according to any one of the preceding claims, wherein said distributed compensation capacitance structure is separated from said resistor arrangement and said substrate by respective insulation layers.

ABSTRACT:



The present invention relates to a frequency-independent voltage divider in which a compensation structure (10) for compensating a distributed parasitic capacitance of a resistor arrangement (20) is arranged between the resistor arrangement (20) and a substrate (50). Thereby, the compensation structure (10) shields the resistor arrangement (20) partly from the substrate (50), and thus shields the parasitic capacitance. This allows for an improved compensation.

Fig. 6

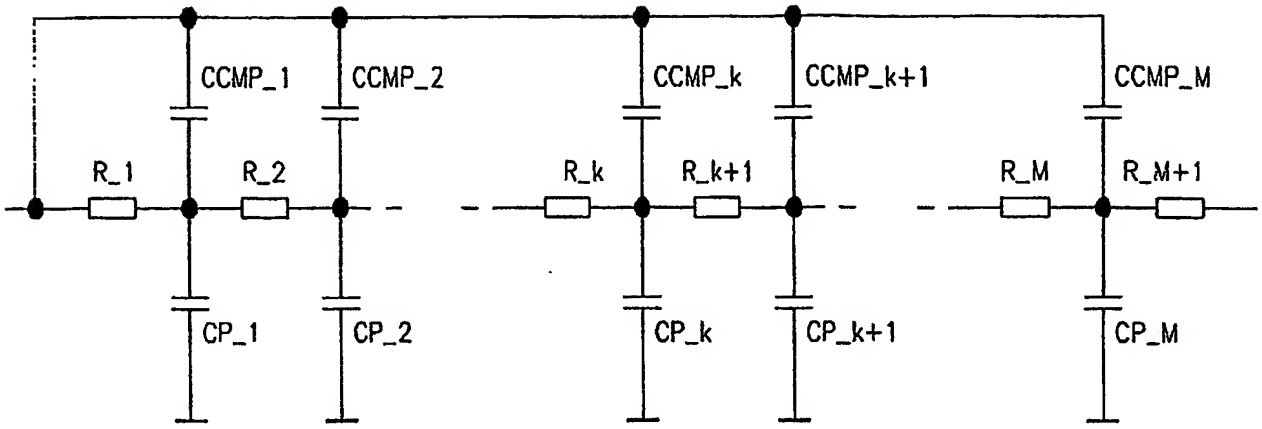
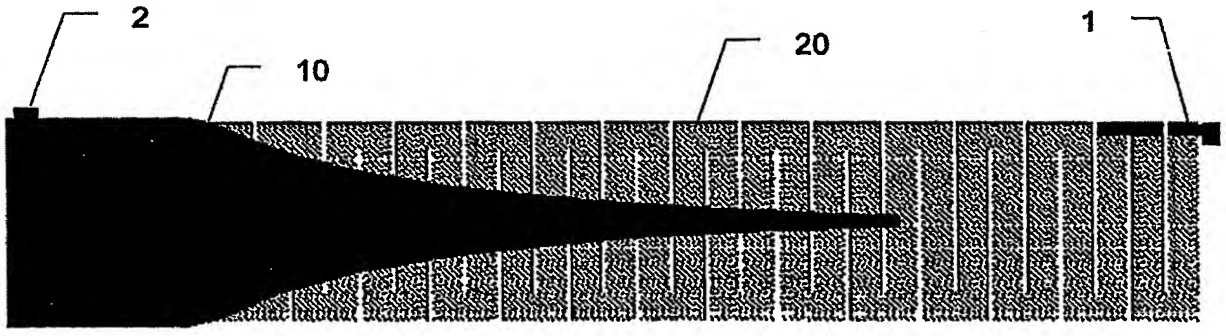
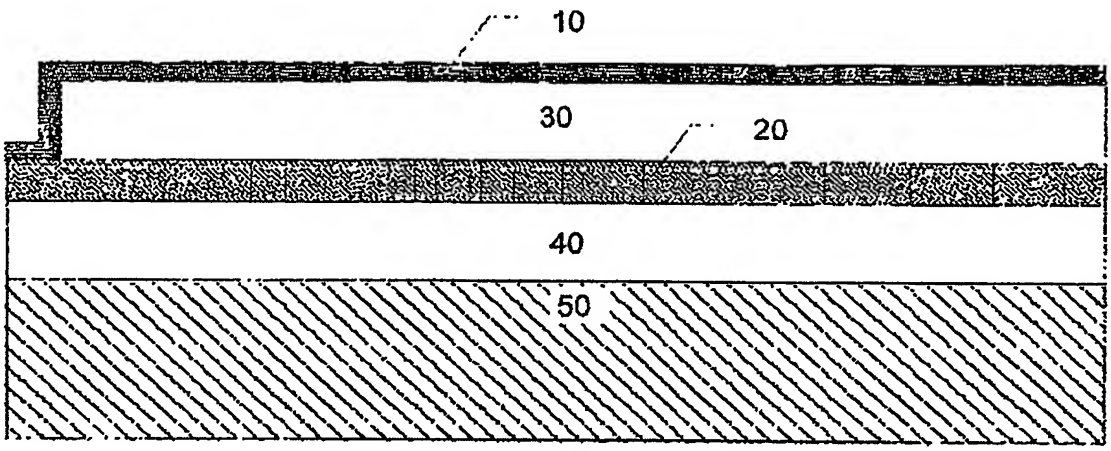



FIG.1




prior art

FIG.2




prior art
FIG.3

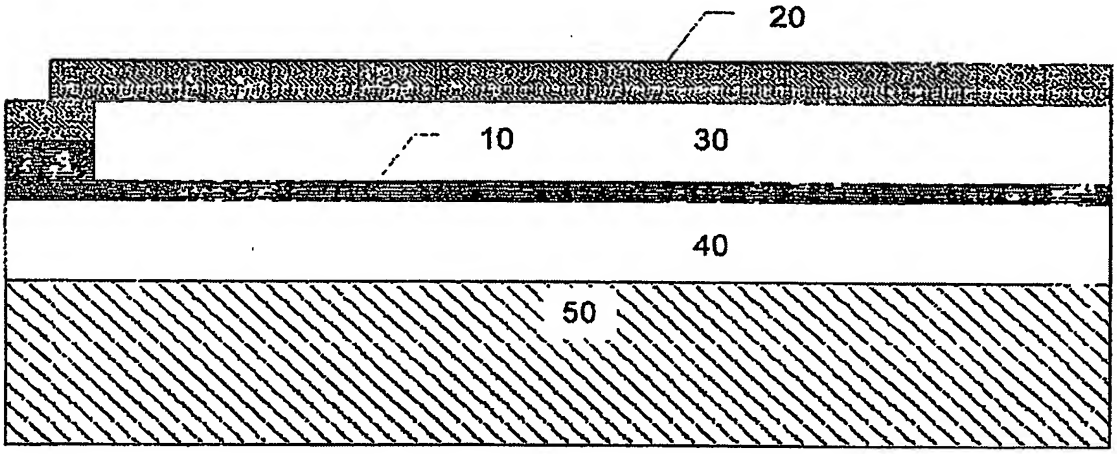



FIG.4

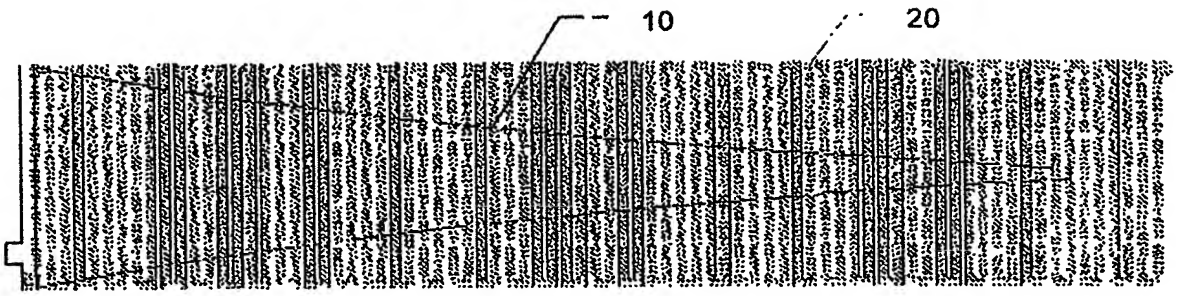



FIG.5

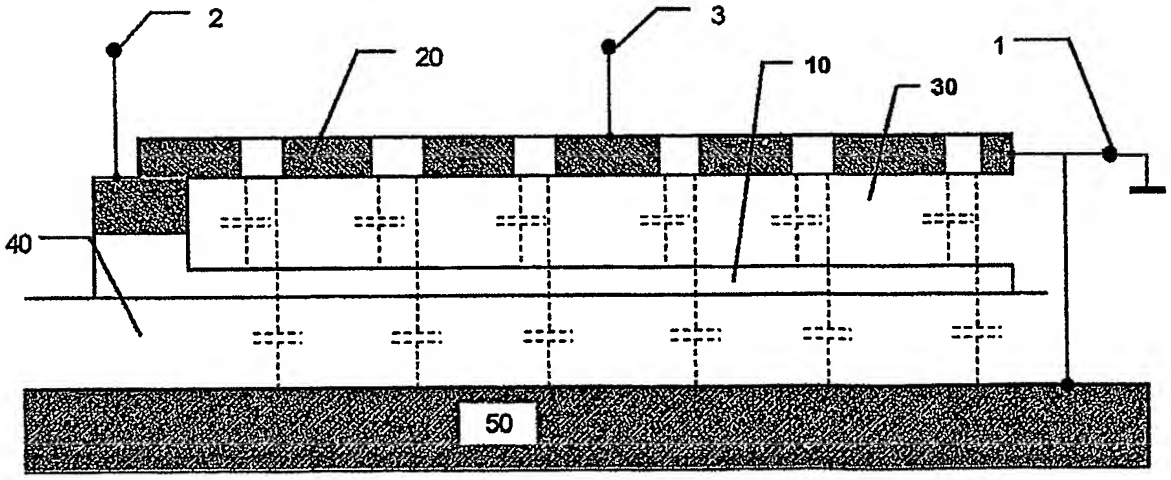



FIG.6